



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,075	11/19/2003	Chandrasekhar Narayan	FIS920030226US1	1074

51872 7590 12/16/2005

LAW OFFICE OF CHARLES W. PETERSON, JR.
FISHKILL
11703 BOWMAN GREEN DR.
SUITE 100
RESTON, VA 20190

EXAMINER

IM, JUNGHWAM

ART UNIT	PAPER NUMBER
----------	--------------

2811

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/707,075	Applicant(s) NARAYAN ET AL.	
	Examiner Junghwa M. Im	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 September 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) 23-28 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 11-22 is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>12/19/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-22 in the reply filed on September 27, 2005 is acknowledged.

Claim Objections

Claim 11 is objected to because of the following informalities: claim 11 recites "said semiconductor substrate" without an antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (US 6448171), hereinafter Wang.

Regarding claims 1, Fig. 4 of Wang shows an integrated circuit (IC) chip [10; col. 6, lines 13-16] with circuits formed thereon, a plurality of chip interconnect pads [12] formed on a surface of said IC chip, one or more of said plurality of chip interconnect pads being an electroplated pad, said electroplated pad having a plated layer [16a, 20, 24] plated to a platable pad.

Art Unit: 2811

Note that “electroplated” is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 2, Fig. 4 of Wang shows an IC chip each said platable pad is disposed in a cavity in a chip surface and said plated layer is formed in said cavity.

Regarding claim 3, Fig. 4 of Wang shows an IC chip said plated layer is a noble metal plated layer (col. 7, line 65 - col. 8, line 8).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Nair et al. (US 6960828), hereinafter Nair.

Regarding claim 4, Fig. 4 of Wang shows most aspect of the instant invention except “said platable pad is a copper/nickel pad.” Fig. 1C of Nair shows a pad [103] formed of copper/nickel pad (col. 6, lines 10-14). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Nair into the device of Wang in order to have the platable pad to be a copper/nickel pad to improve the adhesion between the metal layers.

Regarding claim 5, Fig. 4 of Wang show the noble metal is gold (col. 8, line 1).

Art Unit: 2811

Regarding claims 6 and 7, Fig. 1C of Nair shows an IC chip each said electroplated pad includes a barrier metal layer [115; Ni; col. 7, lines 7-8], said barrier metal layer being a non-platable conductive material layer at the perimeter of said electroplated pad and extending upward along a sidewall of said cavity and alongside said noble metal plated layer.

Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Towle et al. (US Pat. Pub. 2004/0099877), hereinafter Towle

Regarding claim 8, Fig. 4 of Wang show most aspect of the instant invention except "said each plated pad further includes an electrical connection to an underlying strap, said underlying strap extending horizontally from said electrical connection to a chip side wall." Fig. 2 of Towle shows a semiconductor device wherein each pad includes an electrical connection to an underlying strap [22] which extends horizontally from said electrical connection to a chip side wall.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Towle into the device of Wang in order to have each plated pad including an electrical connection to an underlying strap which extends horizontally from said electrical connection to a chip side wall to make a functional connection of two devices.

Regarding claim 9, Fig. 2 of Towle shows said underlying strap extends beyond a crack stop ring [16].

Art Unit: 2811

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang and Towel as applied to claim 8 above, and further in view of Ogawa et al. (us 6566736), hereinafter Ogawa.

Regarding claim 10, the combined teachings of Wang and Towle show most of the claimed structure except "said underlying strap is a tungsten strap." Ogawa discloses that a pad makes a connection to an electrical connection via tungsten contact. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Ogawa into the device of Wang and Towle in order to have said underlying strap made of tungsten to utilize material well known in the art.

Allowable Subject Matter

Claims 11-22 are allowed.

The following is an examiner's statement of reasons for allowance: prior art fails to teach or render obvious a semiconductor device with combinations of elements as set forth in the claims, including in particular a semiconductor wafer comprising a conductive grid line in each kerf space while being connected to a conductive ring and a conductive strap being connected to one of the plurality of chip pads on each chip with each of the plurality of chip pads being connected to one of the conductive straps, each conductive strap being connected to an adjacent conductive grid line, whereby a bias supply current provided to the conductive ring, passes through to each of the plurality of chip pads on said each chip.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

Art Unit: 2811

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

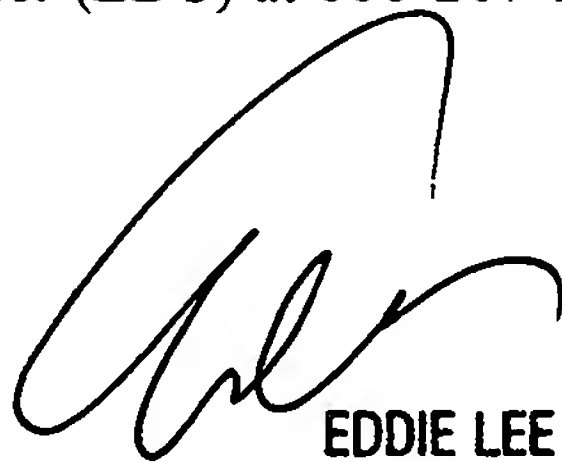
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800